17659

15116

3 Hours / 100 Marks Seat No. | | | | | | | | |

Instructions – (1) All Questions are *Compulsory.*

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

(5) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. a) **Attempt any <u>THREE</u> of the following:** **12**

(i) Define the following terms.

1) Metastability

2) Noise Margin

(ii) Compare BJT and CMOS.

(iii) What is VHDL? State VHDL flow elements.

(iv) Explain flattening and structuring with example.

(v) Explain the estimation of resistance of channel for MOSFET (Sheet Resistance).

Marks

b) **Attempt any ONE of the following:** **6**

(i) Design Melay sequence detector circuit for detecting sequence of '110' using D flip-flop.

(ii) Write VHDL program to Implement JK flip-flop with + ve edge trigger.

(iii) Explain the basic architecture of SPARTAN - 3 FPGA series.

2. Attempt any FOUR of the following: **16**

a) Compare software and hardware description language.

b) Compare FPGA and CPLD.

c) Explain Twin-Tub process in CMOS fabrication.

d) State and explain different operators used in VHDL.

e) Explain different types of simulators.

3. Attempt any FOUR of the following. **16**

a) Design clocked sequential circuit using Toggle flip-flop to count from 00 to 11 (2 bit counter).

b) List the features of FPGA.

c) Write the VHDL code for 3:8 decoder.

d) Explain event scheduling and sensitivity list.

e) Implement the logic circuit using CMOS.

$\gamma = ([A \cdot B] + [C \cdot D])$

Marks

4. a) **Attempt any THREE of the following:** **12**

(i) Explain with syntax.

1) Entity

2) Architecture

(ii) Compare Mealy Machine with Moore Machine.

(iii) Explain sharing of complex operators in VHDL with suitable example.

(iv) Draw and explain working of CMOS Transmission gates.

b) **Attempt any ONE of the following:** **6**

(i) Explain the architecture of Xilinx family of CPLD.

(ii) Write the VHDL code for 8:1 MUX.

(iii) Explain the steps involved in fabrication of n-well process.

5. **Attempt any FOUR of the following:** **16**

a) Draw and Implement the T flip-flop using Moore machine.

b) Define following terms related to fabrication process.

(i) Oxidation

(ii) Diffusion

(iii) Ion - implantation

(iv) Deposition

c) Describe following statement with syntax

(i) Process statement

(ii) Case statement

Marks

d) List the advantages and disadvantages of VHDL.

e) State different coding styles in VHDL and explain any one.

f) Draw the general FPGA chip architecture and explain the same.

6. Attempt any FOUR of the following: **16**

a) Explain product term allocator of Xilinx CPLD family.

b) Write VHDL code for FULL ADDER.

c) State the following data types.

(i) scalar data types

(ii) composite data types

d) Draw HDL design flow for synthesis.

e) Draw and explain working of CMOS Inverter.